

CLAIMS

What Is Claimed Is:

1. A method of caching free cell pointers pointing to memory
5 buffers configured to store data traffic of network
connections, the method comprising:

storing free cell pointers into a pointer random access
memory (RAM), wherein each free cell pointer points
to a memory buffer that is vacant and available for
10 storing data traffic;

temporarily storing at least one free cell pointer into
internal cache configured to assist in lowering a
frequency of reads from and writes to the pointer
RAM;

15 receiving a request from an external integrated circuit
for free cell pointers;

20 sending free cell pointers to queues of the external
integrated circuit, wherein each free cell pointer
in a queue is configured to become a write cell
pointer;

receiving at least one write cell pointer and a
corresponding cell descriptor from the external
integrated circuit; and

25 calculating free cell pointer counter values in order to
keep track of the free cell pointers.

2. The method of Claim 1, wherein the pointer random access memory (RAM) is external to controller circuitry configured to control the steps of the method.

5 3. The method of Claim 1, wherein the external integrated circuit is an egress backplane interface subsystem (EBISS), and the queues of the external integrated circuit are first in, first out (FIFO) queues.

10 4. The method of Claim 1, further comprising sending read cell pointers with corresponding cell descriptors to the external integrated circuit, wherein each read cell pointer points to a memory buffer that has been read and that is free to be reused.

15 5. The method of Claim 1, wherein the step of storing free cell pointers comprises:

storing odd free cell pointers in an odd free list of the pointer RAM; and

20 storing even free cell pointers in an even free list of the pointer RAM.

6. The method of Claim 1, wherein the step of temporarily storing free cell pointers comprises:

storing odd free cell pointers in an odd free space of
internal cache; and

storing even free cell pointers in an even free space of
internal cache.

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7. The method of Claim 4, wherein the step of calculating
free counter values comprises performing at least one of:
incrementing a free counter value to account for a cell
pointer that has been sent to the pointer RAM; and
decrementing a free counter value to account for a cell
pointer that has been received from the pointer RAM.

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8. The method of Claim 1, wherein the step of calculating
free counter values comprises determining that a free
counter value of internal cache is above a high
threshold, and wherein the method further comprises
writing a block of cell pointers in a burst to the
pointer RAM.

- 20 9. The method of Claim 1, wherein the step of calculating
free counter values comprises determining that a free
counter value of internal cache is below a low threshold,
and wherein the method further comprises reading a block
of free cell pointers in a burst from the pointer RAM.

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10. The method of Claim 1, wherein the step of calculating free counter values comprises determining that a free counter value of internal cache is above an overload threshold, and wherein the method further comprises temporarily blocking storing of additional free cell pointers into internal cache.

11. An integrated circuit configured to cache free cell pointers pointing to memory buffers configured to store data traffic of network connections, the integrated circuit comprising:

controller circuitry configured to control operations of:

storing free cell pointers into a pointer random access memory (RAM), wherein each free cell pointer points to a memory buffer that is vacant and available for storing data traffic;

temporarily storing at least one free cell pointer into internal cache configured to assist in lowering a frequency of reads from and writes to the pointer RAM;

receiving a request from an external integrated circuit for free cell pointers;

sending free cell pointers to queues of the external integrated circuit, wherein each free cell pointer in a queue is configured to become a write cell pointer;

receiving at least one write cell pointer and a
corresponding cell descriptor from the external
integrated circuit; and

calculating free cell pointer counter values in
order to keep track of the free cell pointers.

12. The integrated circuit of Claim 11, wherein the pointer
random access memory (RAM) is external to controller
circuitry.

13. The integrated circuit of Claim 11, wherein the external
integrated circuit is an egress backplane interface
subsystem (EBISS), and the queues of the external
integrated circuit are first in, first out (FIFO) queues.

14. The integrated circuit of Claim 11, wherein the
controller circuitry is further configured to control
operation of sending read cell pointers with
corresponding cell descriptors to the external integrated
circuit, wherein each read cell pointer points to a
memory buffer that has been read and that is free to be
reused.

15. The integrated circuit of Claim 11, wherein the operation of storing free cell pointers further configures the controller circuitry to control operations of:

storing odd free cell pointers in an odd free list of the
5 pointer RAM; and

storing even free cell pointers in an even free list of
the pointer RAM.

16. The integrated circuit of Claim 11, wherein the operation of temporarily storing free cell pointers further configures the controller circuitry to control operations of:

storing odd free cell pointers in an odd free space of
internal cache; and

storing even free cell pointers in an even free space of
internal cache.

17. The integrated circuit of Claim 14, wherein the operation of calculating free cell pointer counter values further configures the controller circuitry to control operation of performing at least one of:

incrementing a free counter value to account for a cell
pointer that has been sent to the pointer RAM; and

decrementing a free counter value to account for a cell
25 pointer that has been received from the pointer RAM.

18. The integrated circuit of Claim 11, wherein the operation of calculating free counter values further configures the controller circuitry to control operations of:

5 determining that a free cell pointer counter value of the internal cache is above a high threshold; and
writing a block of cell pointers in a burst to the pointer RAM.

10 19. The integrated circuit of Claim 11, wherein the operation of calculating free counter values further configures the controller circuitry to control operations of:

determining that a free counter value of the internal cache is below a low threshold; and

15 reading a block of free cell pointers in a burst from the pointer RAM.

20 20. The integrated circuit of Claim 11, wherein the operation of calculating free cell pointer counter values further configures the controller circuitry to control operations of:

determining that a free counter value of internal cache is above an overload threshold; and

25 temporarily blocking storing of additional free cell pointers into internal cache.

21. A computer-readable medium carrying one or more sequences of one or more instructions for caching free cell pointers pointing to memory buffers configured to store data traffic of network connections, the one or more sequences of one or more instructions including instructions which, when executed by one or more processors, cause the one or more processors to perform steps of:

storing free cell pointers into a pointer random access memory (RAM), wherein each free cell pointer points to a memory buffer that is vacant and available for storing data traffic;

temporarily storing at least one free cell pointer into internal cache configured to assist in lowering a frequency of reads from and writes to the pointer RAM;

receiving a request from an external integrated circuit for free cell pointers;

sending free cell pointers to queues of the external integrated circuit, wherein each free cell pointer in a queue is configured to become a write cell pointer;

receiving at least one write cell pointer and a corresponding cell descriptor from the external integrated circuit; and

calculating free counter values in order to keep track of
the free cell pointers.

22. The computer-readable medium of Claim 21, wherein the
5 pointer random access memory (RAM) is external to
controller circuitry configured to control operations of
the computer-readable medium.

23. The computer-readable medium of Claim 21, wherein the
external integrated circuit is an egress backplane
interface subsystem (EBISS), and the queues of the
external integrated circuit are first in, first out
(FIFO) queues.

24. The computer-readable medium of Claim 21, wherein the
instructions further cause the processor to perform a
step of sending read cell pointers with corresponding
cell descriptors to the external integrated circuit,
wherein each read cell pointer points to a memory buffer
20 that has been read and that is free to be reused.

25. The computer-readable medium of Claim 21, wherein the
step of storing free cell pointers further causes the
processor to carry out steps of:

storing odd free cell pointers in an odd free list of the
pointer RAM; and

storing even free cell pointers in an even free list of
the pointer RAM.

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26. The computer-readable medium of Claim 21, wherein the
step of temporarily storing free cell pointers further
causes the processor to carry out steps of:

storing odd free cell pointers in an odd free space of
internal cache; and

storing even free cell pointers in an even free space of
internal cache.

27. The computer-readable medium of Claim 24, wherein the
step of calculating free cell pointer counter values
further causes the processor to carry out at least one
of:

incrementing a free cell pointer counter value to account
for a cell pointer that has been sent to the pointer
RAM; and

decrementing a free counter value to account for a cell
pointer that has been received from the pointer RAM.

28. The computer-readable medium of Claim 21, wherein the
step of calculating free counter values further causes

the processor to carry a step of determining that a free counter value of the internal cache is above a high threshold, and wherein the instructions further configure the processor to perform a step of writing a block of cell pointers in a burst to the free pointer RAM.

29. The computer-readable medium of Claim 21, wherein the step of calculating free counter values further causes the processor to carry out a step of determining that a free counter value of the internal cache is below a low threshold, and wherein the instructions further cause the processor to perform a step of reading a block of free cell pointers in a burst from the pointer RAM.

30. The computer-readable medium of Claim 21, wherein the step of calculating free counter values further causes the processor to carry a step of determining that a free counter value of internal cache is above an overload threshold, and wherein the instructions further cause the processor to perform a step of temporarily blocking storing of additional free cell pointers into internal cache.